

**REMARKS**

Claims 1, 2 and 5 are pending in this application. By this Amendment, claims 1, 2 and 5 are amended, and claims 3 and 4 are canceled, without prejudice to or disclaimer of the subject matter recited therein. Support for amendments to claims 1 and 2 can be found at least in Figs. 4B-7C and the corresponding description. Claim 5 is amended for form, and thus is not narrowed by such amendment. Therefore, no new matter is added.

**I. Claims 2 and 5 Satisfy All Formal Requirements**

The Office Action objects to claims 2 and 5 for informalities. Specifically, the Office Action asserts that claim 2 should be amended (1) on line 2 to insert "," between "devices" and "adjacent;" (2) on line 3 to change "the conductive layer" to "a conductive layer;" and (3) on line to change "a conductive layer" to "said conductive layer." The Office Action also asserts that claim 5 should be amended on line 2 to change "an undermost semiconductor device" to "said undermost semiconductor device." By this Amendment, claims 2 and 5 are amended accordingly. Thus, claims 2 and 5 satisfy all formal requirements. Withdrawal of the objection is thus respectfully requested.

**II. The Claims Define Patentable Subject Matter****A. §102(b) Rejection of Claims 1 and 5 over Imaoka**

The Office Action rejects claims 1 and 5 under 35 U.S.C. §102(b) over U.S. Patent No. 5,825,080 to Imaoka et al. (Imaoka). This rejection is respectfully traversed.

Claims 1 and 5 are not anticipated by Imaoka. Imaoka does not disclose "a semiconductor element having first through holes formed therein . . . , each of the electrodes having second through holes formed therein, the second through holes respectively connecting with the first through holes, the second through holes having inner wall surfaces; an insulating film formed on a region including the inner wall surfaces of the second through holes, the insulating film having third through holes respectively inside the second through

holes," as recited in independent claim 1. For example, Imaoka does not disclose the first, second and third through holes, 4, 36 and 50, respectively, as shown in Figs. 4B-7C.

Imaoka only discloses that bumps 15-11 and 17-11 shown in Fig. 6 are electrically connected with each other by an internal wiring electrode 20-11 formed in a through hole or via a hole formed at the semiconductor substrate 14-1 (col. 1, lines 40-45). Thus, Imaoka does not disclose the first, second and third through holes recited in claim 1.

For at least these reasons, claim 1 is patentable over Imaoka. Further, claim 5, which depends from claim 1, is also patentable over Imaoka for at least the reasons discussed above with respect to claim 1, as well as for the additional features it recites. Withdrawal of the rejection is thus respectfully requested.

**B. §102(b) Rejection of Claims 1, 2 and 5 over JP '537**

The Office Action rejects claims 1, 2 and 5 over JP 05-029537 (JP '537). This rejection is respectfully traversed.

Claims 1, 2 and 5 are not anticipated by JP '537. JP '537 does not disclose "a semiconductor element having first through holes formed therein . . . , each of the electrodes having second through holes formed therein, the second through holes respectively connecting with the first through holes, the second through holes having inner wall surfaces; an insulating film formed on a region including the inner wall surfaces of the second through holes, the insulating film having third through holes respectively inside the second through holes," as recited in independent claim 1, and as similarly recited in independent claim 2. For example, JP '537 does not disclose the first, second and third through holes, 4, 36 and 50, respectively, as shown in Figs. 4B-7C.

JP '537 only discloses a semiconductor element 13 having a through hole 5, as shown in Figs 4a and 4b. Further, the insulating layer 15 of JP '537 is formed in the table rear faces

11 and 12 of the chip substrate, and not in the through hole 5 (paragraph [0013]). Thus, JP '537 does not disclose the first, second and third through holes recited in claims 1 and 2.

For at least these reasons, claims 1 and 2 are patentable over JP '537. Further, claim 5, which depends from claim 1, is also patentable over JP '537 for at least the reasons discussed above with respect to claim 1, as well as for the additional features it recites. Withdrawal of the rejection is thus respectfully requested.

**III. Conclusion**

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1, 2 and 5 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



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Date: February 28, 2006

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